REMARKS

Claims 1-34 are currently pending in the application. Claims 1-12, 14, 15, 17-23, 27-31, 33 and 34 were rejected. Claims 13, 16, 24-26 and 32 were objected to. Claims 30, 31, 32 and 34 have been amended.

The Examiner objected to the declaration as being defective. A new declaration has been submitted herewith correcting the defect to which the Examiner referred. The objection is believed addressed thereby.

The Examiner objected to claims 1, 14 and 33 for various informalities. Specifically, the Examiner objected to the limitation in claim 1 which recites:

> sizing transistors in each of the cell instances with reference to an objective function thereby resulting in a first plurality of cell subtypes for each cell type, each cell subtype corresponding to a particular cell type differing from all other cell subtypes corresponding to the particular cell type by at least one transistor dimension.

The Applicants respectfully submit that the limitation is clear on its face.

That is, the limitation describes a portion of the recited method in which the transistors in each cell instance are sized with reference to an objective function. The result of the sizing is that each cell type now includes multiple cell subtypes which differ from each other by "at least one transistor dimension." An exemplary embodiment of this portion of the claimed method may be understood with reference to the present specification beginning at page 25, line 10 to page 26, line 6. In view of the foregoing, the objection is believed addressed.

The Examiner also referred to claim 14 regarding this limitation, but the reason for this is unclear to the Applicants. The Applicants respectfully request clarification of the Examiner's objection to claim 14.

The Examiner objected to claim 33, requesting that the phrase "when executed by a computer" be inserted in the claim. The Applicants do not believe insertion of the requested language to be necessary to render the claim allowable. That is, it is inherent in the claim that

the recited "computer program instructions" which are stored in "at least one computer-readable medium" are, by their very nature, operable "when executed by a computer." In view of this fact, the Applicants do not believe it appropriate to amend the claim as requested.

The Examiner also objected to claims 30, 31, 32 and 34 of being of improper dependent form. The rejection is respectfully traversed.

Each of the claims in question is proper in form in that each is a "product claim that defines the claimed product in terms of the process by which it is made." See MPEP 2173.05(p). In addition, each claimed product embodies, represents, or corresponds to the physical synthesis of a circuit design. That is, as is well known, the term "physical synthesis" in the context of semiconductor circuit design relates to the results of processes by which design information (e.g., a circuit schematic) is translated into a form which may be employed to manufacture the physical product. The physical embodiment of any such translated information may be classified as a "device, apparatus, manufacture, or composition of matter," and may also, therefore, be properly claimed as a product-by-process.

Notwithstanding the foregoing, claims 30, 31, 32 and 34 have been amended to explicitly relate the claimed products to the "physical synthesis" recited in the preamble of claim 1. The Applicants respectfully submit that these claims are proper product-by-process claims, and that therefore the objection should not be maintained.

The Examiner rejected claim 31 under 35 U.S.C. 101 as being directed to non-statutory subject matter. Specifically, the Examiner stated that "[d]ata structures...are not statutory if not claimed as embodied (executed) in computer-readable media." The rejection is respectfully traversed.

Claim 31 recites "At least one computer readable medium having data structures stored therein representing a sized netlist" (emphasis added). That is, contrary to the Examiner's assertion, the claim explicitly recites data structures stored in at least one computer readable

medium. Therefore, the claim cannot be declared "not statutory" for the reason the Examiner sets forth. Furthermore, the recited data structures represent a netlist which has been optimized to achieve "a balance between the objective function and a cost associated with maintaining the selected subtypes distinct." Thus, because such data structures are embodied in at least one computer-readable medium, the claim is directed to statutory subject matter. See In re Lowry 32 F.3d 1579, 1583-84, 32 USPQ2d 1031, 1035 (Fed. Cir. 1994) (claim to data structure that increases computer efficiency held statutory).

Finally, as stated in the Examination Guidelines for Computer-Related Inventions available on the USPTO web site (http://www.uspto.gov/web/offices/com/hearings/software/analysis/computer.html), "a claimed computer-readable medium encoded with a data structure defines structural and functional interrelationships between the data structure and the medium which permit the data structure's functionality to be realized, and is thus statutory." In view of the foregoing, the Applicants respectfully request withdrawal of the rejection.

The Examiner rejected claims 31 under 35 U.S.C. 112, second paragraph, for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. In view of the foregoing, the rejection is believed overcome.

The Examiner rejected claims 1-6, 9, 11, 14, 15, 17-23, 27, 28, 30, 33 and 34 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Application Publication 2002/0023255 (Karniewicz). The rejection is respectfully traversed.

Karniewicz describes a hierarchical semiconductor design which includes several levels of abstraction (Abstract). In referring to Figs. 1(a)-1(c), Karniewicz describes four levels of a hierarchical semiconductor test structure. Fig. 1(a) shows two levels of the hierarchy, one being the so-called "higher level cells" 100, 110 and 112, and the other being the lowest level of the hierarchy, so-called "basic atom cells" 102-108 in higher level cell 100, 114-118 in higher level

cell 110, and 120-130 in higher level cell 112. See paragraphs [0026]-[0028].

Fig. 1(b) introduces another level to the hierarchy, referred to as the "device" level, which includes devices 132 and 140. Device 132 includes three higher order cells 134-138, and device 140 includes two higher order cells 142 and 144. Finally Fig. 1(c) introduces the fourth and highest level of the hierarchy, the semiconductor test structure 146 which includes three devices 148-152. See paragraphs [0030]-[0035].

While Karniewicz does refer to the changing of parameters (e.g., size and placement) associated with various cells in the hierarchy, it does so merely to make the point that such changes are propagated to affected cells on other levels of the hierarchy (e.g., see paragraphs [0027] and [0031]).

Karniewicz does not, however, teach the sizing of transistors for each of a plurality of cell instances such that each cell type is divided into a plurality of subtypes. Neither does it teach the merging of selected subtypes such that the number of subtypes for at least one cell type is reduced. Finally, it does not teach such a merging step as achieving "a balance between the objective function and a cost associated with maintaining the selected subtypes distinct." Because Karniewicz does not teach any of these limitations, it cannot be said to anticipate the invention as recited in claim 1. In addition, it cannot be said to anticipate or obviate any claims dependent on claim 1 for at least the reasons discussed. The Applicants invite the Examiner to identify portions of any of the cited references which teach these aspects of the claimed invention.

The Examiner rejected claims 7, 8, 10, 12, 16 and 24 under 35 U.S.C. 103(a) as being unpatentable over Karniewicz in view of U.S. Patent No. 6,445,065 (Gheewala). The Examiner also rejected claims 29 and 31 under 35 U.S.C. 103(a) as being unpatentable over Karniewicz in view of U.S. Patent No. 5,790,415 (Pullela). In view of the foregoing discussion regarding claim 1, the rejections are believed overcome for at least the reasons discussed.

The Examiner objected to claims 13, 16, 24, 25 and 26 as being dependent on rejected base claims, but indicated the claims would be allowable if rewritten in independent form. The Applicants respectfully acknowledge the Examiner's indication of allowable subject matter. However, in view of the foregoing discussion regarding claim 1, the Applicants believe the claims to which the Examiner objects are allowable in their current form.

In view of the foregoing, Applicants believe all claims now pending in this application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested. If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (510) 843-6200.

Respectfully submitted,
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